JC03 Rec'd PCT/PTO 30 JAN 2002

FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
218251US6XPCT	
U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	
10/030157	

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR00/02065	18 July 2000	30 July 1999

TITLE OF INVENTION

METHOD OF FABRICATING THROUGH-CONNECTIONS IN A SUBSTRATE, AND SUBSTRATE EQUIPPED WITH SUCH CONNECTIONS

APPLICANT(S) FOR DO/EO/US

ROBERT Philippe

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (24) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☒ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☐ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

PCT/IB/304/Application Data Sheet (2 Pages)
PCT/IB/308/Drawings (3 Sheets)
Notice of Priority/Form PTO-1449
Amended Sheets (Pages 13, 14 and 15)

U.S. APPLICATION NO (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/030157	PCT/FR00/02065	218251US6XPCT

24. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1040.00	
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00	
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $740.00	
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) $710.00	
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00	
	ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00
	Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	$0.00

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	10 - 20 =	0	x $18.00	$0.00	
Independent claims	2 - 3 =	0	x $84.00	$0.00	
Multiple Dependent Claims **(check if applicable)**.			☐	$0.00	
	TOTAL OF ABOVE CALCULATIONS =			$890.00	
☐	Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.			$0.00	
	SUBTOTAL =			$890.00	
	Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +			$0.00	
	TOTAL NATIONAL FEE =			$890.00	
☐	Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			$0.00	
	TOTAL FEES ENCLOSED =			$890.00	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of **$890.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **15-0030** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Surinder Sachar
Registration No. 34,423

22850

Surinder Sachar
SIGNATURE

Gregory J. Maier
NAME

25,599
REGISTRATION NUMBER

Jan 30 2002
DATE

218251US-154-154-6-X-PCT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

ROBERT PHILIPPE : ATTN: APPLICATION DIVISION

SERIAL NO: NEW U.S. PCT APPLN :
(Based on PCT/FR00/02065)

FILED: HEREWITH : EXAMINER:

FOR: METHOD OF FABRICATING :
THROUGH-CONNECTIONS A
SUBSTRATE, AND SUBSTRATE
EQUIPPED WITH SUCH CONNECTIONS

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to a first examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel Claims 1-10 without prejudice.

Please add new Claims 11-20 as follows:

11. (New) A method of fabricating conducting through-connections between a front face and a rear face of a substrate, comprising:

hollowing into the substrate, from the rear-face side, cavities having a depth and a cross-section which are defined so as to delimit, by these cavities, studs of defined cross-section configured to provide for electrical conduction between the front and rear faces;

filling in the cavities with a dielectric material to insulate the stud from a rest of the substrate and to integrate the stud with the substrate;

hollowing the front face of the substrate opposite each stud so as to make each stud show through and thus convert each stud into a conducting through-connection; and

physically forming points of contact opposite each face of each stud showing through by depositing a conducting material, insulated from the substrate, on each of these faces.

12. (New) The method of fabricating conducting through-connections between the front face and the rear face of a substrate as claimed in claim 11, wherein the filling of the cavities comprises:

depositing the dielectric material in the cavities; and

removing, from a surface of the substrate, overflows of the deposit of dielectric material by thinning the rear face of the substrate until the studs are uncovered.

13. (New) The method of fabricating conducting through-connections between the front face and the rear face of a substrate as claimed in claim 11, further comprising, after delimiting the studs and before filling in the cavities:

metallizing the studs by depositing a conducting layer on the studs.

14. (New) The method of fabricating conducting through-connections between the front face and the rear face of a substrate as claimed in claim 13, wherein the filling-in of the cavities comprises:

depositing the dielectric material in the cavities;

removing, from a surface of the substrate, overflows of the deposit of the dielectric material by thinning the rear face of the substrate until the studs are uncovered; and

removing the conducting layer from the surface of the substrate, by thinning of the metallized faces of the substrate.

15. (New) The method of fabricating conducting through-connections between the front face and the rear face of a substrate as claimed in claim 11, further comprising:

thinning the substrate until the dielectric material contained in the cavities is uncovered so as to make the studs show through on the front face of the substrate.

16. (New) The method of fabricating conducting through-connections between the front face and the rear face of a substrate as claimed in claim 11, further comprising:

hollowing the front face of the substrate opposite each stud until the dielectric material contained in the cavities is reached, so as to make the studs show through on the front face of the substrate.

17. (New) The method of fabricating conducting through-connections between the front face and the rear face of a substrate as claimed in claim 11, wherein the physical formation of the points of contact comprises:

depositing an insulating layer on a same side as the faces of the studs showing through;

opening up a contact region opposite each face of the studs showing through by masking and etching of the insulating layer;

depositing a conducting layer on the same side as the faces of the studs showing through; and

cutting out the points of contact by masking and etching of the conducting layer.

18. (New) The method of fabricating conducting through-connections between the front face and the rear face of a substrate as claimed in claim 11, wherein the dielectric filling material is glass.

19. (New) A substrate of silicon equipped with conducting through-connections between its front face and its rear face, wherein the conducting through-connections are silicon studs extending over an entire height of the substrate and are surrounded by a

dielectric material which delimits the studs and keeps the studs integral with the substrate, the studs showing through on the front and rear faces of the substrate, and points of contact being formed opposite each face showing through of each stud by a conducting material insulated from the substrate.

20. (New) The substrate as claimed in claim 19, wherein the silicon studs are coated over their entire height by a conducting metallization itself surrounded by the dielectric material.

IN THE ABSTRACT

Please delete the original Abstract page 16 in its entirety and insert therefor:

ABSTRACT

A method of fabricating conducting through-connections in a substrate, and a substrate equipped with such connections. The method of fabricating conducting through-connections between the front face and the rear face of a substrate hollows into the substrate, from the rear-face side, cavities having a depth and a cross-section that are defined so as to delimit studs of defined cross-section, which are intended to provide for electrical conduction between the front and rear faces, and filling in the cavities with a dielectric material. The substrate is equipped with conducting through-connections between its front face and its rear face. The conducting connections are provided by way of studs delimited by cavities filled in with a dielectric material. Such a method and substrate may find application, in particular, to substrates used for the fabrication of microsensors.

REMARKS

Favorable consideration of the above-identified application, as presently amended, is respectfully requested.

The present preliminary amendment is submitted to place the above-identified application in more proper format under United States practice.

By the present preliminary amendment Claims 1-10 are cancelled and new Claims 11-20 are presented for examination. New Claims 11-20 are deemed to be self-evident from the original disclosure, and thus are not deemed to raise any issues of new matter. New Claims 11-20 have been written to not recite any reference numerals, to be more in more proper format under United States practice, and to no longer recite the term "consisting" by instead reciting the broader term "comprising". New Claims 11-20 are not believed to be narrower than Claims 1-10 in any aspect and are believed to only broaden the scope of the claims.

A new Abstract believed to be in more proper format under United States practice is also submitted herein.

The present application is believed to be in condition for a full and thorough examination on the merits. An early and favorable consideration of the present application is hereby respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Attorney of Record
Registration No. 25,599
Surinder Sachar
Registration No. 34,423

22850

(703) 413-3000
Fax No.: (703)413-2220
SNS/rac
I:\atty\SNS\218251US-PR.wpd

218251US-154-154-6-X-PCT

Marked-Up Copy
Serial No: _____
Amendment Filed on:
1-30-2002

IN THE CLAIMS

Claims 1-10 (Cancelled).

Claims 11-20 (New).

IN THE ABSTRACT

Abstract (New).

I:\atty\SNS\218251US-PR.wpd

Method of fabricating through-connections in a substrate, and substrate equipped with such connections

The invention relates to a method of fabricating conducting through-connections between the front face and the rear face of a substrate, as well as a substrate equipped with such conducting connections.

The invention applies especially to substrates intended to accommodate a microelectronics structure, such as a sensor, a magnetic head or a microactuator, or intended to accommodate a microelectronics circuit.

The substrate may be electrically conducting (for example made of silicon, or of polysilicon) or insulating (for example made of ceramic).

The conducting through-connections make it possible to provide discrete electrical contacts between the front face and the rear face of a semiconducting, insulating or conducting substrate.

The use of conducting through-connections makes it possible:

- to have a denser number of electrical contacts,
- to provide electrical contacts over a stack of substrates,
- to supply the components electrically from the rear face of the substrate when the wiring cannot be done on the front face.

The technique widely used to fabricate these conducting connections consists in piercing the substrate from front to back (for example by laser firing), in electrically insulating the hole (in the case of a semiconducting or conducting substrate) and in filling in the hole with a conducting material.

In the majority of applications, the filling of the holes has to be complete in order to allow the electrical contact to be picked up easily, in order to continue the technological stages relating to the front and rear faces after the fabrication of the conducting connections and in order to allow the electrical

contact to be taken up after any thinning of the substrate at the end of the process.

The filling is generally done with a conducting paste injected under pressure (method used to form microelectronics packages). Although effective, this technique is fairly "violent" and gives rise to defects on the faces of the substrate (splinters, roughness, cracks, stresses, etc). This technique can even entail a loss of insulation in the case of semiconducting substrates. Furthermore, the paste is made up of metallic particles mixed with a solution based on polymers and solvents. This solution, which serves as a binder, has to be removed after filling. This removal causes a not inconsiderable shrinkage of the conducting material which can be the origin of holes which are responsible for loss of conduction. The paste may also be the origin of contamination, the polymers being difficult to remove.

Other techniques have been envisaged, in particular those described in the document "Electrical Interconnections Through Semiconductor Wafers" by T. R. Anthony, published in the magazine Journal Application of Physic 52(8) of August 1981. It covers:

- the use of electrolysis methods, which generally lead to a surface filling of the hole due to problems of wetting and of edge effects or

- the filling by a molten metal. This technique poses problems of thermal expansion. Metals with a low melting point (below the softening temperature of the substrate) exhibit a high coefficient of thermal expansion, often much higher than the substrate. This results in difficulties of a mechanical nature (stresses) or technological nature (risk of cracking of the deposited layers).

One of the objects of the invention is to alleviate the abovementioned drawbacks.

To that end, the subject of the invention is a method of fabricating conducting through-connections

between the front face and the rear face of a substrate. The method consists:

- in hollowing into the substrate, from the rear-face side, cavities having a depth and a cross section which are defined so as to delimit studs of defined cross section which are intended to provide for electrical conduction between the two faces and
- in filling in the cavities with a dielectric material.

A further subject of the invention is a substrate equipped with conducting through-connections between its front face and its rear face. The conducting connections consist of studs delimited by the hollowing of cavities, in the rear face of the substrate. These cavities are filled in with a dielectric material.

The method consists in forming the conducting through-connections by delimiting in the substrate (semiconducting, insulating or conducting substrate) studs which will serve as conducting passages between the rear face and the front face of the substrate. The delimiting is performed by hollowing out cavities. The cavities are filled in with a dielectric material in order to provide for the mechanical strength and the electrical insulation of the studs.

The use of an insulant as a material for filling the hollowed cavities presents the advantage of offering a coefficient of thermal expansion close to that of the substrates widely used in microelectronics.

Furthermore, after filling, a thinning of the substrate on the two faces makes it possible to remove the short circuits due to the substrate and the surpluses of filling material.

The invention moreover has the advantage that it allows:

- easy picking-up of the electrical contact, even after thinning of the substrate, and
- very good electrical insulation of the conducting passages.

The substrate may be insulating (for example of ceramic) or slightly conducting (for example of lightly doped semiconductor). In these cases a metallic deposit is formed or can be formed on the studs before filling of the cavities in order to provide the electrical conductivity of the studs.

In the case of the use of a silicon substrate of silicon-on-insulator type, better known by the acronym SOI, the thinning of the substrate which is intended to cut the short circuits after filling can be replaced by etching of the silicon and oxide layers on the front-face side in order to make the studs show through.

A substrate equipped with conducting through-connections which are obtained by a method according to the invention can play a part in delimiting an enclosure. The substrate may make it possible to seal the enclosure in such a way that the atmosphere in the enclosure is perfectly defined with, in particular, a pressure capable of being used as a reference pressure. The leaktightness of the substrate is not in any way affected by the conducting through-connections consisting of the studs. This is because, on the one hand, the conducting through-connections obtained by a method according to the invention leave the front face of the substrate perfectly flat and, on the other hand, the dielectric material fills in the cavity in a completely hermetic way. The possibility of being able to carry out sealing plays a vital role, in particular for the fabrication of microsensors.

Other characteristics and advantages of the invention will emerge with the aid of the description which follows. The description is given with regard to the annexed figures which represent:

- Figure 1, a substrate on completion of a first stage of the method,
- Figure 2, a magnification of a stud,
- Figure 3, a substrate on completion of a second stage of the method,

- Figure 4, a substrate on completion of a third stage of the method,

- Figure 5, a substrate on completion of a fourth stage of the method,

- Figure 6, a substrate on completion of a fifth stage of the method,

- Figure 7, a substrate on completion of a sixth stage of the method,

- Figure 8, a substrate on completion of a seventh stage of the method,

- Figures 9 to 14, the stages of the method implemented with a substrate consisting of a stack of layers.

Figure 1 represents a substrate 1 having a front face 2 and a rear face 3. The substrate 1 is usually of silicon, but it may be of another type, ceramic for example. The method according to the invention applies equally well to a slightly conducting substrate (a semiconductor such as silicon, possibly doped), and to an insulating (ceramic) substrate or else to a conducting substrate.

The first stage of the method consists in delimiting studs 4 in the substrate 1. These studs 4 are intended to provide an electrical connection through the substrate 1. The studs 4 are advantageously formed in the substrate 1 itself.

The delimiting of a stud 4 is performed by hollowing out a cavity 5 in the rear face 3 of the substrate 1. According to the example of Figure 1, the cavity 5 has a ring-shaped circular cross section. This ring has a width I_d and a diameter $2\times(I_p+I_d)$ with a solid part of diameter $2\times I_p$ which constitutes the stud. The cavity 5 has a depth Pd less than the thickness e of the substrate 1. The cross section of the cavity 5 may not be circular, but square, rectangular, etc. The same goes for the cross section of the stud 4, the cross section of the stud possibly being of a different shape to that of the cavity.

The hollowing of a cavity 5 is achieved by known techniques. One of the known techniques consists, with the aid of a mask, for example, made of resin or of oxide, in carrying out dry anisotropic etching. Another known technique consists, with the aid of a mask, in carrying out chemical etching. For a silicon substrate of thickness e = 525 μm, the depth P_d of the cavity 5 is of the order of 300 μm. For a ceramic substrate, the hollowing is generally performed by mechanical machining of the substrate.

Figure 2 is a magnification of a stud. The stud 4, of diameter $2\times I_p$, is delimited by the cavity 5 in the shape of a cylindrical ring of width I_d. For example, the stud 4 has a diameter $2\times I_p$ = 50 μm and the cavity 5 a width I_d = 50 μm.

Figure 3 illustrates the second stage of the method. This second stage is optional; it is necessary when the substrate 1 is not sufficiently conducting, for example in the case of a ceramic substrate. This stage consists in carrying out the depositing of a thin conducting layer 6 which has the function of increasing the conductivity of the stud. Depending on the technique used to carry out the deposition, the layer 6 is deposited only on the rear face or else simultaneously on the two faces.

The technique used should allow a deposition over the entire height P_d of the stud. On completion of this stage, the surface of the rear face, and possibly of the front face, is completely covered with a thin conducting layer; the surface of the rear face comprising the surface of the studs 4 as far as the bottom of the cavities 5. A technique of chemical deposition in vapor phase, for example of tungsten (W), makes it possible to obtain a deposition of a conducting layer 6 in accordance with the above description. Such a technique is known by the acronym CVD, an abbreviation of the term Chemical Vapor Deposition.

Figure 4 illustrates the third stage of the method. The cavities 5 are filled in with a defined material 7. The material 7 should be insulating or only slightly conducting in order to insulate the stud from the rest of the substrate 1 when the latter is conducting. The deposition technique consists typically in deposition by melting. The method makes it possible to use materials having a low coefficient of thermal expansion. The material may advantageously have a coefficient of thermal expansion very close to that of the silicon, in the case of a silicon substrate, while having a melting temperature less than that of the silicon. The low coefficient of thermal expansion makes it possible to avoid the awkward problems relating to the difference in coefficient of thermal expansion between the filling material and the substrate; problems with which certain known connection techniques are confronted.

The material adopted may be glass, deposited by melting.

The material 7, in addition to an insulation function which is necessary when the substrate is conducting, performs a function of retention of the stud 4. The material 7 integrates the stud 4 over its height with the substrate 1. The material 7 may, moreover, participate in delimiting a sealed enclosure.

Depending on the deposition techniques used, the material deposited may cover the whole of the rear face as Figure 4 illustrates.

Figure 5 illustrates the fourth stage of the method.

This stage makes it possible to uncover the substrate by removing the unwanted surface layers. When the dielectric 7 overflows from the cavities 5, it has to be removed by thinning the rear face 3 of the substrate 1. The thinning may consist of a lapping, polishing, etching or a combination of these various techniques. Lapping consists in abrasion which has the drawback of leaving a surface having a scratched

surface state. In order to remedy this drawback, the abrasion is followed by polishing in order to obtain a smooth surface state. One polishing technique is widely known by the acronym CMP, an abbreviation of the term Chemical Mechanical Planarization. This technique has a double effect, mechanical and chemical, which makes it possible to obtain a smooth surface. The polishing is particularly important when the second stage has not been implemented, that is to say when there has been no deposition of a conducting layer. The etching may consist of dry or wet etching. Dry etching employs a plasma, wet etching employs a chemical bath.

The thinning described above may make it possible to remove the conducting layer (deposited during the second stage) from the rear face 3 and from the front face 2 if the conducting layer is present on the latter. The removal of the conducting layer can be carried out in an independent or supplementary way by a known specific technique, for example by dry etching or wet etching. The dry etching may be of the RIE type, an abbreviation of the term Reactive Ion Etching.

On completion of the fourth stage, the substrate comprises a set of studs 4. This set may comprise a single stud 4. The maximum density of studs capable of being delimited in a substrate of given size depends, in particular, on the performance of the etching technique used during the first stage. The cavities 5, filled in with a dielectric material 7, provide the mechanical strength and the electrical insulation of the studs 4. The material 7 may, moreover, participate in delimiting a sealed enclosure. The use of a dielectric as a material for filling the hollowed cavities presents the advantage of offering a coefficient of thermal expansion similar to that of the substrates widely used in microelectronics. The method makes it possible to solve the problems relating to the difference in coefficient of thermal expansion between the substrate and the filling material. The method

overcomes problems of removal and of contamination, moreover.

The fifth stage, Figure 6, makes it possible to eliminate the short circuit between the stud 4 and the front face 2 of the substrate 1. The elimination is performed by a thinning of the front face according to a known technique. A first technique may consist in lapping, by abrasion, the front face 2 of the substrate 1; a second technique may consist of dry or wet etching; a third technique may consist of a combination of lapping, etching and polishing. The studs 4, possibly metallized 6, are conducting elements which make it possible to establish electrical through-connections between the two faces 2, 3 of the substrate 1. The front face 2 of the substrate 1 is generally intended for the installation of an electronic function or of a microstructure, a microsensor for example. The studs 4 make it possible, for example, to supply the microsensor electrically via the rear face 3 by providing an electrical connection between the rear face 3 and points of contact within the circuit of the microsensor. The studs 4 make it possible to have available contact points which do not affect the flatness of the surface of the front face 2 of the substrate 1. A substrate 1, equipped with studs 4 obtained according to a method according to the invention, may contribute to delimiting an enclosure. The substrate may make it possible to achieve sealing of the enclosure in such a way that the atmosphere in the enclosure is perfectly defined with, in particular, a pressure possibly being used as a reference pressure. The leaktightness of the enclosure is not in any way affected by the conducting through-connections consisting of the studs. In fact, on completion of the fifth stage, the front face 2 of the substrate 1 is perfectly flat.

The sixth stage, Figure 7, consists in depositing a thin insulating layer 8 on the two faces 2, 3 of the substrate 1 and in opening up contact

regions 9 opposite the studs 4. The deposition of a thin insulating layer 8 is performed by a known technique, for example of the plasma type such as the technique known by the acronym PECVD, an abbreviation of the term Plasma Enhance Chemical Vapor Deposition.

The opening of the contact regions 9 can be performed by masking and etching of the insulating layer 8. The masking can be carried out by photolithography.

The seventh stage, Figure 8, consists in physically forming the points 10 of contact opposite the studs 4. The physical forming is carried out by known techniques which consist in depositing a thin conducting layer 11 on the two faces 2, 3 of the substrate 1 and in cutting out the points 10, for example by masking and etching of the conducting layer 11. The masking can be carried out by photolithography.

Figures 9 to 14 illustrate an implementation of the method with a substrate consisting of a stack of layers. This substrate 1 may be of SOI type, an abbreviation of the term Silicon On Insulator. The first layer 12 of the stack consists of silicon. The free face of the first layer corresponds to the rear face 3 of the substrate. The second layer 13 of the stack is an insulating layer. It consists of a silicon oxide. The third layer 14 of the stack consists of silicon. Its free face corresponds to the front face 2 of the substrate. An SOI substrate has the following thicknesses, for example:

1^{st} layer: 500 µm

2^{nd} layer: 0.4 µm

3^{rd} layer: from 0.2 µm to several µm.

The third layer 14 is generally reserved for the fabrication of electronic functions or for the implementation of microstructures, for example a microsensor, a microactuator, etc.

Figure 9 illustrates the first stage of the method. According to this implementation, the cavities

5 are hollowed until the insulating layer 13 is uncovered.

When the method is implemented with a substrate of SOI type, the second stage does not exist.

Figure 10 illustrates the third stage of the method. The type of substrate does not alter the implementation of the third stage; this stage progresses according to the description given with regard to Figure 4.

Figure 11 illustrates the fourth stage of the method. The type of substrate does not alter the implementation of the fourth stage; this stage progresses according to the description given with regard to Figure 5.

When the method is implemented with a substrate consisting of a stack of layers, in particular of the SOI type, the fifth stage does not exist.

Figure 12 illustrates the sixth stage of the method. Given that the studs 4 are not visible on the front face 2, the depositing of the thin insulating layer 8 is performed only on the rear face 3. The depositing progresses according to the description given with regard to Figure 7, with, as a limitation, a deposition on the rear face 3.

Figure 13 illustrates the seventh stage of the method. The implementation is different from that described with regard to Figure 8 to the extent that the points 10 of contact are present only on the rear face 3.

In order to obtain a through-stud, supplementary stages are necessary. They are illustrated by Figure 14. They consist:

- in etching the third layer 14 and the second layer 13 from the front face 2 by using a mask. The etching is carried out as far as the stud 4, according to a technique identical to that described with regard to Figure 1, in order to uncover the stud and only a part of the dielectric.

- in physically forming the points 10 of contact on the front face 2 according to a technique similar to that described with regard to Figure 13. In the case of the points 10 of contact on the front face, the cross section of etching of the insulating layer 8 is less than the cross section of etching of the third and second layers of the substrate.

ART 34 AMDT

CLAIMS

1. A method of fabricating conducting through-connections between the front face (2) and the rear face (3) of a substrate (1), characterized in that it comprises the stages consisting:

- in hollowing into the substrate (1), from the rear-face (3) side, cavities (5) having a depth (P_d) and a cross-section which are defined so as to delimit, by these cavities, studs (4) of defined cross-section which are intended to provide for electrical conduction between the two faces (2, 3),

- in filling in the cavities (5) with a dielectric material (7) in order to insulate the stud from the rest of the substrate and in order to integrate the stud with the substrate,

- in hollowing the front face of the substrate opposite each stud so as to make it show through and thus convert the stud into a conducting through-connection,

- and in physically forming the points (10) of contact opposite each face of each stud (4) showing through by depositing a conducting material (11), insulated from the substrate, on each of these faces.

2. The method of fabricating conducting through-connections between the front face (2) and the rear face (3) of a substrate (1) as claimed in claim 1, characterized in that the filling of the cavities (5) consists:

- in depositing the dielectric material (7) in the cavities (5),

- in removing, from the surface of the substrate (1), the overflows of the deposit of dielectric material (7) by thinning the rear face (3) of the substrate (1) until the studs (4) are uncovered.

3. The method of fabricating conducting through-connections between the front face (2) and the rear face (3) of a substrate (1) as claimed in claim 1,

characterized in that it consists, after delimiting the studs (4) and before filling in the cavities (5):

- in metallizing the studs (4) by depositing a conducting layer (6) on the studs.

4. The method of fabricating conducting through-connections between the front face (2) and the rear face (3) of a substrate (1) as claimed in claim 3, characterized in that the filling-in of the cavities (5) consists:

- in depositing the dielectric material (7) in the cavities (5),

- in removing, from the surface of the substrate (1), the overflows of the deposit of the dielectric material (7) by thinning the rear face (3) of the substrate (1) until the studs (4) are uncovered,

- in removing the conducting layer (6) from the surface of the substrate (1), by thinning of the metallized faces (2, 3) of the substrate (1).

5. The method of fabricating conducting through-connections between the front face (2) and the rear face (3) of a substrate (1) as claimed in any one of claims 1 to 4, characterized in that it consists:

- in thinning the substrate (1) until the dielectric material contained in the cavities (5) is uncovered so as to make the studs (4) show through on the front face (2) of the substrate (1).

6. The method of fabricating conducting through-connections between the front face (2) and the rear face (3) of a substrate (1) as claimed in either of claims 1 and 2, characterized in that it consists:

- in hollowing the front face (2) of the substrate (1) opposite each stud until the dielectric material (7) contained in the cavities (5) is reached, so as to make the studs (4) show through on the front face (2) of the substrate (1).

7. The method of fabricating conducting through-connections between the front face (2) and the rear face (3) of a substrate (1) as claimed in one of claims

1 to 6, characterized in that the physical formation of the points (10) of contact consists:

- in depositing an insulating layer (8) on the same side (2, 3) as the faces of the studs (4) showing through,

- in opening up a contact region (9) opposite each face of the studs (4) showing through by masking and etching of the insulating layer (8),

- in depositing a conducting layer (11) on the same side (2, 3) as the faces of the studs (4) showing through,

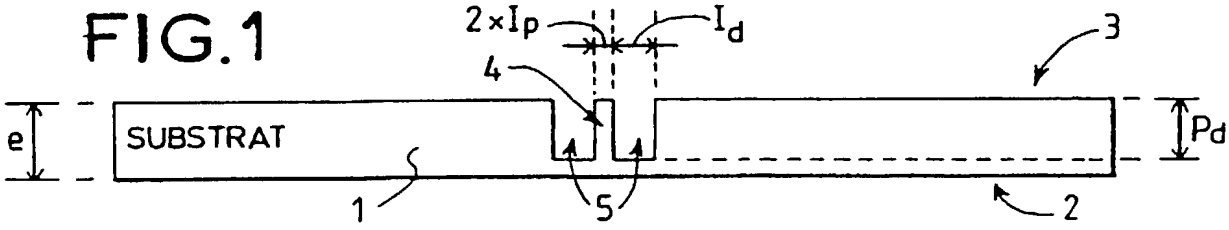
- in cutting out the points (10) of contact by masking and etching of the conducting layer (11).

8. The method of fabricating conducting through-connections between the front face (2) and the rear face (3) of a substrate (1) as claimed in any one of claims 1 to 7, characterized in that the dielectric filling material (7) is glass.

9. A substrate (1) of silicon equipped with conducting through-connections between its front face (2) and its rear face (3), characterized in that the conducting connections are silicon studs extending over the entire height of the substrate and are surrounded by a dielectric material which delimits them and keeps them integral with the substrate, these studs showing through on the two faces of the substrate, and points of contact being formed opposite each face showing through of each stud by a conducting material insulated from the substrate.

10. The substrate as claimed in claim 9, characterized in that the silicon studs are coated over their entire height by a conducting metallization itself surrounded by the dielectric material.

FIG.1



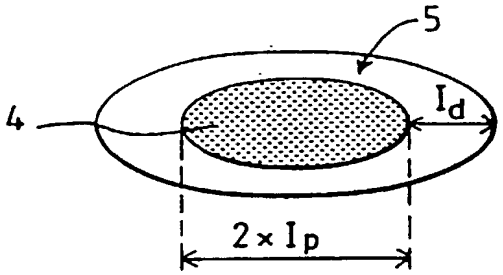


FIG.2

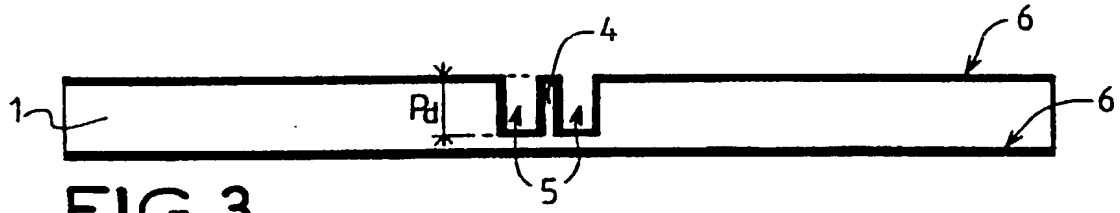


FIG.3

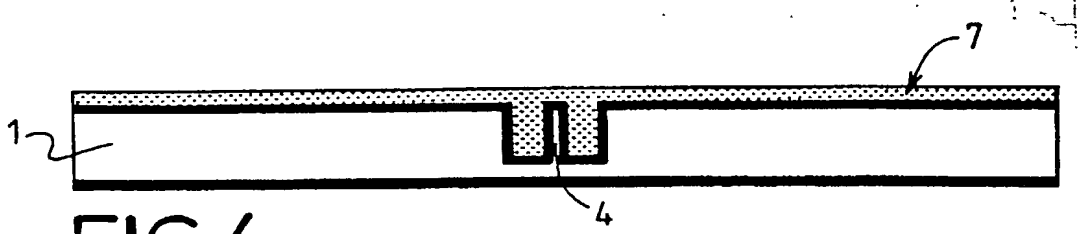


FIG.4

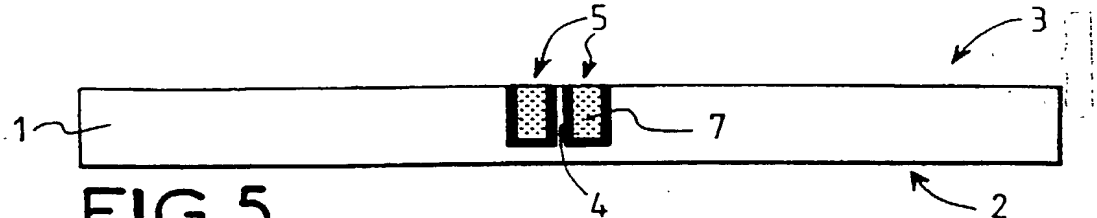


FIG.5

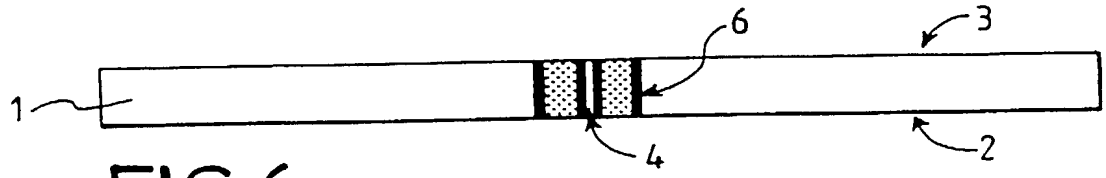


FIG.6

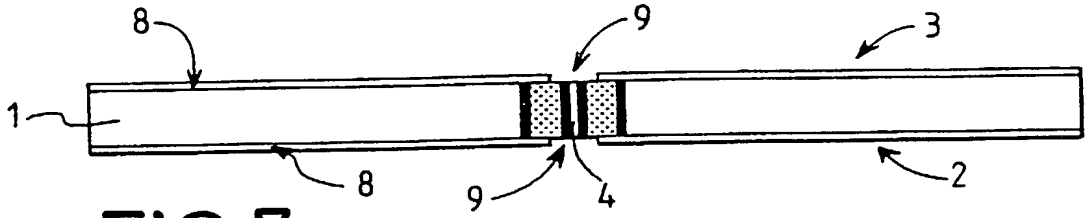


FIG.7

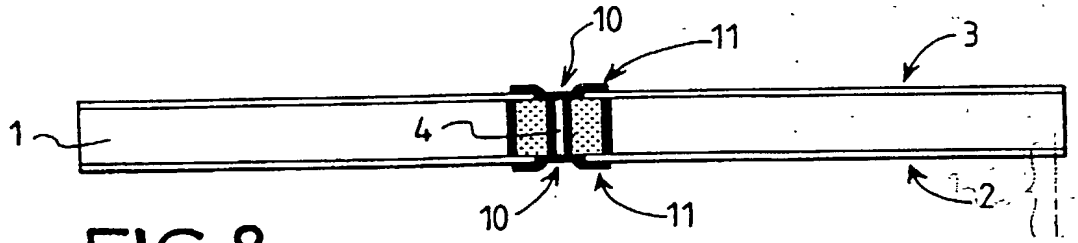


FIG.8

FIG.13

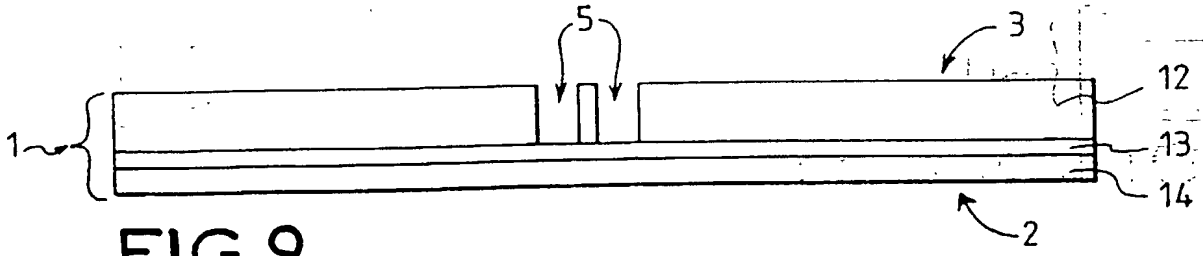


FIG.9

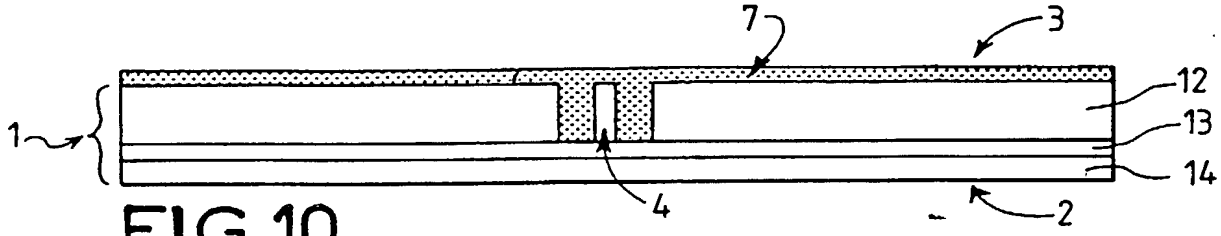


FIG.10

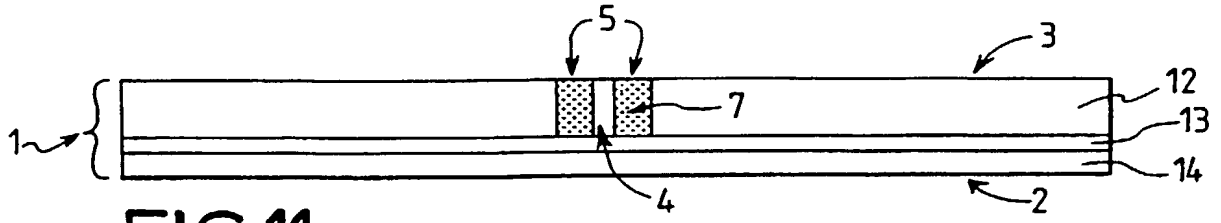


FIG.11

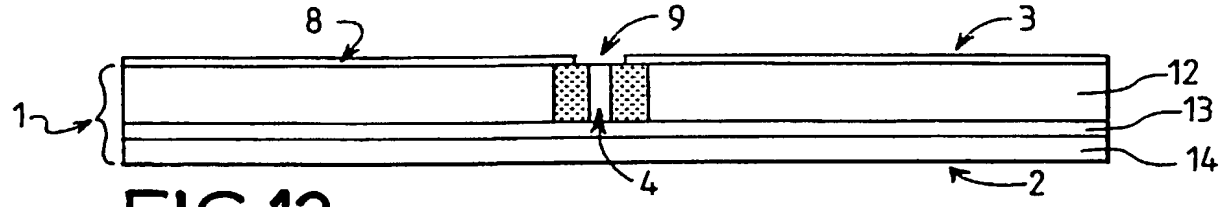


FIG.12

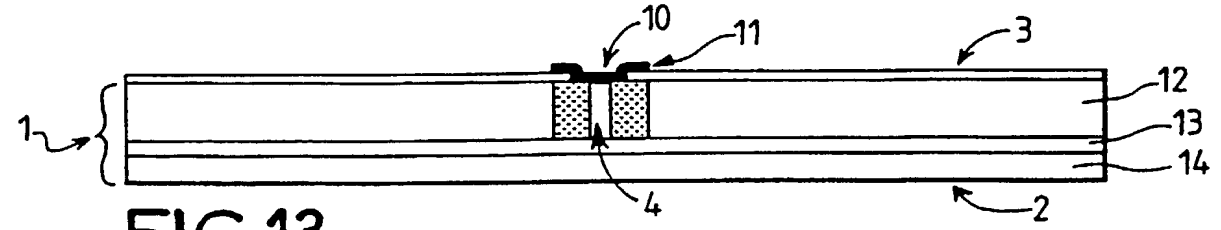


FIG.13

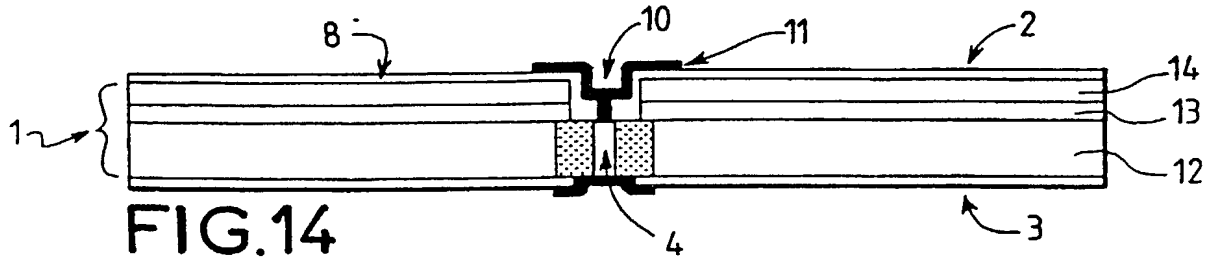


FIG.14

Declaration and Power of Attorney for Patent Application
Déclaration et Pouvoirs pour Demande de Brevet

French Language Declaration

En tant l'inventeur nommé ci-après, je déclare par le présent acte que:

Mon domicile, mon adresse postale et ma nationalité sont ceux figurant ci-dessous à côté de mon nom.

Je crois être le premier inventeur original et unique (si un seul nom est mentionné ci-dessous), ou l'un des premiers co-inventeurs originaux (si plusieurs noms sont mentionnés ci-dessous) de l'objet revendiqué, pour lequel une demande de brevet a été déposée concernant l'invention intitulée

et dont la description est fournie ci-joint à moins

☐ ci-joint

☐ a été déposée le _____

sous le numéro de demande des Etats-Unis ou le numéro de demande international PCT

_____ et modifiée le

_____ (le cas échéant).

Je déclare par le présent acte avoir passé en revue et compris le contenu de la description ci-dessus, revendications comprises, telles que modifiées par toute modification dont il aura été fait référence ci-dessus.

Je reconnais devoir divulguer toute information pertinente à la brevetabilité, comme défini dans le Titre 37, § 1.56 du Code fédéral des réglementations.

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

METHOD OF FABRICATING THROUGH-CONNECTIONS I A SUBSTRATE, AND SUBSTRATE EQUIPPED WITH SUCH CONNECTIONS

the specification of which

☐ is attached hereto.

☒ was filed on **July 18, 2000**

as United States Application Number or PCT International Application Number

PCT/FR00/02065 and was amended on

_____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

French Language Declaration

Je revendique par le présent acte avoir la priorité étrangère, en vertu du Titre 35, § 119(a)-(d) ou § 365(b) du Code des Etats-Unis, sur toute demande étrangère de brevet ou certificat d'inventeur ou, en vertu du Titre 35, § 365(a) du même Code, sur toute demande internationale PCT désignant au moins un pays autre que les Etats-Unis et figurant ci-dessous et, en cochant la case, j'ai aussi indiqué ci-dessous toute demande étrangère de brevet, tout certificat d'inventeur ou toute demande internationale PCT ayant une date de dépôt précédant celle de la demande à propos de laquelle une priorité est revendiquée.

I hereby claim foreign priority under Title 35, United States Code, § 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
Demande(s) de brevet anterieure(s) dans un autre pays.

(Number) (Numéro)	(Country) (Pays)	(Day/Month/Year Filed) (Jour/Mois/Anné de dépôt)	Priority Claimed Droit de priorité Revendiqué Yes Oui	No Non
99 09938	**FRANCE**	**30 JULY 1999**	☒	☐
			☐	☐

Je revendique par le présent acte tout bénéfice, en vertu du Titre 35, § 119(e) du Code des Etats-Unis, de toute demande de brevet provisoire effectuée aux Etats-Unis et figurant ci-dessous.

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

(Application No.) (Nº de demande)	(Filing Date) (Date de dépôt)

Je revendique par le présent acte tout bénéfice, en vertu du Titre 35, § 120 du Code des Etats-Unis, de toute demande de brevet effectuée aux Etats-Unis, ou en vertu du Titre 35, § 365(c) du même Code, de toute demande internationale PCT désignant les Etats-Unis et figurant ci-dessous et, dans la mesure où l'objet de chacune des revendications de cette demande de brevet n'est pas divulgué dans la demande antérieure américaine ou internationale PCT, en vertu des dispositions du premier paragraphe du Titre 35, § 112 du Code des Etats-Unis, je reconnais devoir divulguer toute information pertinente à la brevetabilité, comme défini dans le Titre 37, § 1.56 du Code fédéral des réglementations, dont j'ai pu disposer entre la date de dépôt de la demande antérieure et la date de dépôt de la demande nationale ou internationale PCT de la présente demande:

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application No.) (Nº de demande)	(Filing Date) (Date de dépôt)	(Status: Patented, Pending, Abandoned) (Statut : breveté, en cours d'examen, abandonné)
PCT/FR00/02065	**JULY 18, 2000**	

Je déclare par le présent acte que toute déclaration ci-incluse est, à ma connaissance, véridique et que toute déclaration formulée à partir de renseignements ou de suppositions est tenue pour véridique; et de plus, que toutes ces déclarations ont été formulées en sachant que toute fausse déclaration volontaire ou son équivalent est passible d'une amende ou d' une incarcération, ou des deux, en vertu de la § 1001 du Titre 18 du Code des Etats-Unis, et que de telles déclarations volontairement fausses risquent de compromettre la validité de la demande de brevet ou du brevet délivré à partir de celle-ci.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

French Language Declaration

POUVOIRS: En tant que l'inventeur cité, je désigne par la présente l'(les) avocat(s) et/ou agent(s) suivant(s) pour qu'ils poursuive(nt) la procédure de cette demande de brevet et traite(nt) toute affaire s'y rapportant avec l'Office des brevets et des marquees: *(mentionner le nom et le numéro d'enregistrement).*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number)*

Norman F. Oblon, Reg. No. 24,618; Marvin J Spivak, Reg. No. 24,913; C. Irvin McClelland, Reg. No. 21,124; Gregory J Maier, Reg No.25,599; Arthur I Neustadt, Reg. No. 24,854; Richard D. Kelly, Reg. No. 27,757, James D Hamilton, Reg No. 28,421, Eckhard H. Kuesters, Reg No. 28,870; Robert T. Pous, Reg. No 29,099; Charles L. Gholz, Reg. No. 26,395; Vincent J. Sunderdick, Reg No. 29,004; William E. Beaumont, Reg. No. 30,996; Steven B. Kelber, Reg No. 30,073; Robert F. Gnuse, Reg. No. 27,295; Jean-Paul Lavalleye, Reg No. 31,451; Stephen G. Baxter, Reg. No. 32,884; Martin M. Zoltick, Reg. No. 35,745; Robert W. Hahl, Reg. No 33,893, Richard L Treanor, Reg. No. 36,379; Steven P. Weihrouch, Reg. No. 32,829; John T Goolkasian, Reg. No 26,142; Marc R. Labgold, Reg. No. 34,651; William J. Healey, Reg No. 36,160; Richard L. Chinn, Reg. No. 34,305; Steven E. Lipman, Reg. No. 30,011; Carl E. Schlier, Reg. No. 34,426; James J Kulbaski, Reg. No. 34,648; Catherine B. Richardson, Reg. No. 39,007; Richard A. Neifeld, Reg. No. 35,299; and J. Derek Mason, Reg. No. 35,270, with full powers of substitution and revocation.

Addresser toute correspondance à:

Send Correspondence to:
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VIRGINIA 22202 U.S.A

Adresser tout appel téléphonique à.
(nom et numéro de téléphone)

Direct Telephone calls to: *(name and telephone number)*

(703) 413-3000

Nom complete de l'unique ou premier inventeur	Full name of sole or first inventor Philippe ROBERT January 3, 2002
Signature de l'inventeur Date	Inventor's signature Date Philippe Robert
Domicile	Residence 26100 ROMANS FRANCE
Nationalité	Citizenship French
Adresse Postale	Post Office Address 8, rue Bonneveaux
	26100 ROMANS FRANCE
Nom complete du second co-inventeur, le cas echeant	Full name of second joint inventor, if any
Signature de l'inventeur Date	Second inventor's signature Date
Domicile	Residence
Nationalité	Citizenship
Adresse Postale	Post Office Address

(Fournier les mêmes renseignements et la signature de tout co-inventeur supplémentaire)

(Supply similar information and signature for third and subsequent joint inventors)